

n-Type Behavior of Graphene Supported on Si/SiO₂ Substrates

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Graphene is a one-atom-thick sheet of carbon with the atoms arranged in a two-dimensional (2D) honeycomb configuration. The electronic band structure¹ and phonons² in this interesting 2D system were predicted theoretically many years ago. However, graphene was produced in the laboratory only recently: first, by Novosolev *et al.*³ by the micromechanical cleavage of a single sheet from graphite, and second, by de Heer *et al.*⁴ by the thermal decomposition of SiC in high vacuum. The electronic energy bands are constructed primarily from atomic p_z orbitals that are perpendicular to the sheet. The conduction and valence bands touch at the so-called “Dirac points” in the six corners of the hexagonal Brillouin zone and form an unusual zero-gap semiconductor with linear band dispersion. Many interesting electronic properties have been reported for graphene, including the fractional quantum Hall effect^{5–7} and minimum quantum conductivity.⁵

Being, in essence, an all-surface material, graphene also proves extremely sensitive to its environment, that is, the supporting substrate and/or gases and chemicals that might be on the graphene surface. Though the influence of the substrate^{8,9} and adsorbed molecules^{10,11} has been addressed previously in different ways in the literature, the exact role that each of them plays is not yet fully understood. Differences are observed between graphene samples placed on the same substrate and between samples placed on different substrates.

It has also been suggested that the low-temperature mobility of the carriers in graphene is determined by scattering from charged impurities at the surface of the SiO₂.^{8,9} Supporting this idea, recent experiments show that graphene flakes sus-

ABSTRACT Results are presented from an experimental and theoretical study of the electronic properties of back-gated graphene field effect transistors (FETs) on Si/SiO₂ substrates. The excess charge on the graphene was observed by sweeping the gate voltage to determine the charge neutrality point in the graphene. Devices exposed to laboratory environment for several days were always found to be initially p-type. After ~20 h at 200 °C in ~5 × 10⁻⁷ Torr vacuum, the FET slowly evolved to n-type behavior with a final excess electron density on the graphene of ~4 × 10¹² e/cm². This value is in excellent agreement with our theoretical calculations on SiO₂, where we have used molecular dynamics to build the SiO₂ structure and then density functional theory to compute the electronic structure. The essential theoretical result is that the SiO₂ has a significant surface state density just below the conduction band edge that donates electrons to the graphene to balance the chemical potential at the interface. An electrostatic model for the FET is also presented that produces an expression for the gate bias dependence of the carrier density.

KEYWORDS: graphene · Si/SiO₂ substrate · silicon dioxide structure · charge transfer · field effect transistors · chemical doping

ended above the substrate have a factor of 10 higher mobility (2 × 10⁵ cm²/V · s) than those supported by the substrate.^{12,13} Experiments also seem to reveal a very important role played by the substrate on the morphological structure.^{14,15} STM measurements suggest that single layer graphene follows the corrugations of the SiO₂ substrate,¹⁴ and experiments on graphene nanoelectromechanical systems indicate that the substrate induces significant stress in few-layer graphene samples.¹⁵

In this paper, we report experimental and theoretical studies of graphene supported on Si substrates with a thermally grown oxide. The Si substrate is highly doped and also serves as a gate electrode. By studying the electrical properties of graphene on SiO₂ in a high vacuum, we were able to remove adsorbed gases deposited under ambient conditions in the laboratory that render the graphene p-type. After extended desorption of these gases, the system becomes n-type. Theoretical

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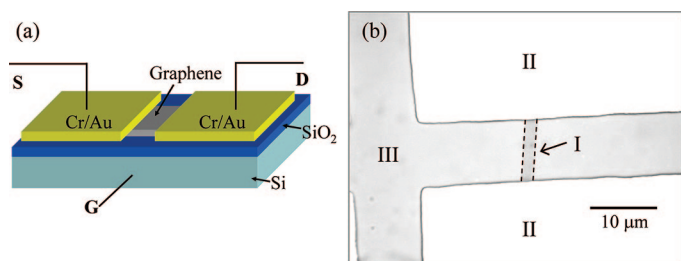


Figure 1. (a) Graphene device supported on SiO₂ with underlying doped Si serving as the back gate (G); S and D refer to the source and drain contacts. (b) Optical micrograph of a graphene device fabricated with TEM grids as a shadow mask. The graphene flake is $\sim 3 \mu\text{m}$ wide. The following areas can be identified on the optical image: (I) single graphene layer (also indicated with dashed lines), (II) Cr/Au electrodes, and (III) SiO₂ dielectric.

calculations are also presented here that indicate that this n-type behavior is intrinsic to the SiO₂/graphene interface; that is, surface states on SiO₂ are donating electrons to the graphene.

RESULTS AND DISCUSSION

A schematic drawing of our back-gated graphene FET supported on a SiO₂/Si substrate is shown in Figure 1 together with an optical micrograph of the device. The optical image shows two square Cr–Au contacts deposited over each end of a rectangular graphene flake of dimensions $\sim 13 \mu\text{m} \times 3 \mu\text{m}$. Since our device fabrication scheme involves shadow-masking to make electrical contacts, it therefore has the advantage that it is a photo-resist-free process. A glass fiber has also been reported as a successful shadow mask for graphene.¹⁶ We believe that employing e-beam or photolithographic resists and solvents while patterning electrical contacts unnecessarily exposes the graphene surface to chemicals (e.g., poly(methyl methacrylate) resin, solvents, etc.). These chemicals may prove difficult to remove later.¹⁴

The electronic band structure of graphene near the Fermi level (E_g) is somewhat unique. Near-mirror image valence and conduction bands touch each other at the six corners (K, K' points) of a 2D Brillouin zone. These band contact points are commonly called Dirac points,³ and the nomenclature stems from the linear dispersion of the electronic band energy E with two-dimensional wave vector k , (i.e., $E = \pm \hbar v_F k$), where v_F is the Fermi velocity. Thus the charge carriers in graphene behave like photons (massless particles) but travel at a velocity v_F much less than the speed c of light (i.e., $v_F \sim c/300$).^{5,6}

Using the well-known expression for the density of states per unit area for linear bands in a two-dimensional system (i.e., $g(E) = g_s g_v E/2\pi \hbar^2 v_F^2$), where the spin degeneracy $g_s = 2$ and the valley degeneracy $g_v = 2$, the position of E_g in the graphene is related to the graphene charge density n by the relation $E_g = \hbar v_F \sqrt{\pi \cdot n}$, where it is understood that free-standing perfect graphene has $E_g = 0$.

According to a simple model proposed earlier for a graphene FET, we can write the net charge density in graphene (n) in terms of the gate potential V_g (cf. Appendix)

$$n = \frac{\epsilon \epsilon_0}{e d_s} (V_g - V_{\text{Dirac}}) \quad (1)$$

where $\epsilon \epsilon_0$ and d_s are, respectively, the gate dielectric permittivity and thickness, e is the charge of the electron, and V_{Dirac} is a constant related to the net charge n_0 on the graphene when $V_g = 0$ (i.e., $V_{\text{Dirac}} = -n_0 e d_s / \epsilon \epsilon_0$). Graphene in its pristine state should have $n_0 = 0$. However, chemical charge transfer between graphene and the substrate or with adsorbed gases can create negative or positive n_0 ; the condition $n = 0$ is then reached through the application of $V_g = V_{\text{Dirac}}$. Theoretically, we find that surface states of SiO₂ pin the Fermi level at ~ 0.5 eV below the SiO₂ conduction band edge. Thus, we consider a model where the surface states mediate the Dirac voltage. As shown in the Appendix, the Dirac voltage can be expressed as follows:

$$V_{\text{Dirac}} = \left(\frac{e \beta d_s}{\epsilon \epsilon_0} + 1 \right) \frac{(W_g - W)}{e} - \frac{(W_m - W)}{e} \quad (2)$$

where β is the density of surface states per unit area on the SiO₂ surface, W_g , W_m , and W are the work functions of graphene, p-doped Si, and SiO₂, respectively. The goal of this study is to experimentally determine n_0 and to learn to what extent n_0 can be identified with charge transfer between SiO₂ and graphene.

From eq 1, sweeping the gate voltage induces a transition between electron and hole conduction when $V_g = V_{\text{Dirac}}$. In terms of the electronic states, this is equivalent to sweeping the Fermi level E_g through the Dirac point in the p_z (or π) electronic density of states, that is, the charge neutrality point. When E_g is at this point, the electronic density of states is very small (or zero) and a peak should be observed in the drain–source resistance $R_{\text{ds}}(V_g)$ curves. This is the so-called “Dirac peak”.

Our graphene FETs were exposed to ambient conditions for several days before electrical characterization. They are almost always observed to be p-type ($n_0 > 0$); that is, the Dirac peak in R_{ds} was found at a significantly positive V_g (i.e., $+50 \text{ V} < V_g < +100 \text{ V}$). A positive Dirac peak of the same order of magnitude is not uncommon in graphene devices on SiO₂ substrates.^{3,17,18} We observed that this p-doping could slowly be reversed by vacuum-annealing at $T \sim 200$ °C at $\sim 5 \times 10^{-7}$ Torr, suggesting that the p-doping stems from adsorption of ambient gas molecules that remove electrons from the graphene. The time evolution of the Dirac peak during the first 20 h of the vacuum-annealing process at $T = 200$ °C is shown in Figure 2. As can be seen, the peak shifts rapidly over the first 90

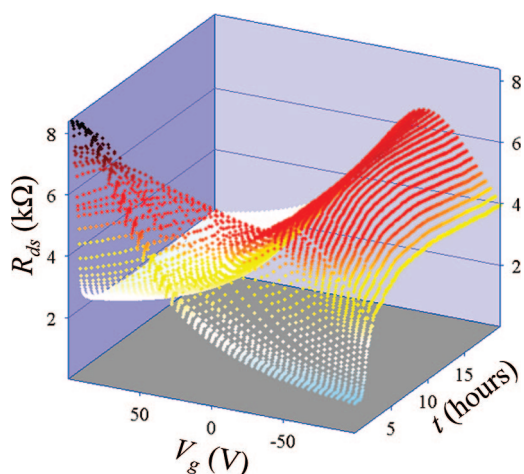


Figure 2. Time evolution of the source–drain resistance R_{ds} versus V_g curves at $T = 200$ °C during the first 20 h of vacuum-annealing of the graphene FET device shown schematically in Figure 1. Initially, the peak in R_{ds} (Dirac peak) is out of range ($V_g > 100$ V); after ~ 5 h, the Dirac peak appears at negative V_g and evolves slowly to the final position at $V_g \sim -50$ V.

min from $V_g \sim +100$ V to $V_g \sim 0$ V, then moves more slowly to a final value at negative gate bias (i.e., $V_g \sim -48$ V). The graphene FET is now decidedly n-type.

In panels a and b in Figure 3, we plot, respectively, the time evolution and the value of R_{ds} at the Dirac peak maximum as well as the position (V_{Dirac}) of the Dirac peak. The evolution is observed during the initial heat treatment at 200 °C (first 28 h) and later after the temperature is suddenly lowered to 25 °C; the data for $R_{ds}(V_{\text{Dirac}})$ are plotted normalized to the initial value of $R_{ds}(V_{\text{Dirac}}) = R_0$ at $t = 0$. The behavior is rather interesting. Initially (cf. Figure 3a), the normalized maximum resistance R_{ds}/R_0 can be observed to drop rapidly during the first ~ 2 h to a minimum at $R_{ds}/R_0 \sim 0.65$, and then recover more slowly (over ~ 6 h) to the degassed, equilibrium value $R_{ds}/R_0 \sim 0.75$ at $T = 200$ °C. At $t = 28$ h, the temperature of the device was lowered suddenly to 25 °C; one can observe a slow recovery of $R_{ds}/R_0 \sim 1$ that takes place over ~ 5 h. Our anticipated behavior under these conditions was a slow evolution from the initial value $R_{ds}/R_0 \sim 1$ to a lower “degassed” value, but without the undershoot effect in Figure 3a, and we have no clear understanding of this observation. We have observed this same undershoot effect for other similar graphene FETs degassed at 200 °C in Ar as well as in H_2 atmospheres. The decrease in R_{ds}/R_0 with annealing is also interesting because, if one considers degassing to only “undope”

the graphene, R_{ds}/R_0 would have been expected to increase. The decrease of R_{ds}/R_0 (at fixed T) suggests a decrease in scattering due to degassing, that is, the removal of H_2O and/or O_2 , N_2 , etc. After long-term degassing at 200 °C, the observed increase in the equilibrium value of R_{ds}/R_0 with decreasing temperature (i.e., $R_{ds}/R_0 \sim 0.75$ at 200 °C increasing to $R_{ds}/R_0 \sim 1$ at 25 °C) suggests a drop in carrier concentration as the Fermi function sharpens at E_g . This increase must overcome the decrease in the phonon scattering contribution. Our observed T dependence of $R_{ds}(V_{\text{Dirac}})$ is consistent with previous experimental results.^{19–22} These earlier reports did not offer an explanation for the observed monotonic reduction in $R_{ds}(V_{\text{Dirac}})$ with increasing T , but rather focused on the behavior of $R_{ds}(T)$ away from the neutrality point which the authors tentatively identified with static impurities,¹⁹ static ripples,²⁰ or surface phonon scattering.²²

In Figure 3b, we plot the position of the Dirac peak maximum during vacuum-annealing, first for 28 h at 200 °C, then during 22 h at 25 °C. Note that the peak has shifted from ~ -48 V to ~ -27 V after the device cools. The time dependence shown in Figure 3b is also interesting and resembles the form shown in Figure 3a for R_{ds}/R_0 . Whereas R_{ds}/R_0 emphasizes the interplay between the width of the Fermi Dirac function, carrier scattering, and carrier concentration, the peak position $V_g = V_{\text{Dirac}}$ emphasizes the net charge on the graphene. Except for the undershoot effect, the decrease of V_{Dirac} at 200 °C with t (Figure 3b) is not unexpected. Upon degassing, a decrease in hysteresis in the electrical properties was reported previously for nanotube FETs and identified with the removal of charge trapping by adsorbed H_2O molecules, more specifically, H_2O bound to the SiO_2 gate dielectric.²³ These authors found that pumping in vacuum at room temperature was ineffective, but heating in dry environments to $T \geq 200$ °C was much more successful in removing the adsorbant.²³ We further suspect that O_2 may be weakly chemisorbing to graphene, as well, thereby acting as an acceptor

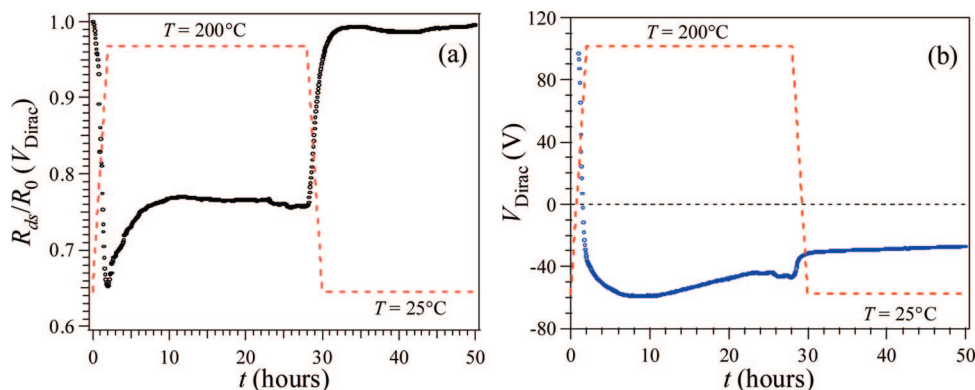


Figure 3. Time evolution of (a) the normalized maximum value of the $R_{ds}(V_g)$ curves, that is, the normalized amplitude of the Dirac peak, $R_{ds}(V_{\text{Dirac}})/R_0$, and (b) the Dirac voltage (V_{Dirac}) for a typical graphene FET supported on $\text{SiO}_2/\text{p}^+\text{Si}$. The dashed line indicates the time evolution of the temperature during the vacuum-degassing experiment, that is, $T = 200$ °C for the first ~ 28 h, whereupon the temperature is suddenly changed to $T = 25$ °C (in both cases, the chamber pressure was maintained at $\sim 5 \times 10^{-7}$ Torr).

(i.e., p-doping the system). This view is consistent with our work on carbon nanotube films.²⁴

An interesting effect, shown in Figure 3b, is the rapid change of the V_{Dirac} observed at $t = 28$ h when the temperature is lowered from 200 to 25 °C, indicating a reduction of the n-doping of the graphene with temperature (and after a long-term degassing). We will address this change in $V_{\text{Dirac}}(T)$ below after describing our theoretical model. However, an explanation of this observation may be beyond the scope of our current theoretical model.

We next turn to theoretical calculations in support of the experimental observation of n-type behavior in fully degassed graphene FETs supported on Si/SiO₂. We will argue that the n-type behavior observed is associated with a low work function for SiO₂ relative to graphene. We determine the expected intrinsic exchange of charge between SiO₂ and graphene when realistic atomic configurations of SiO₂ are considered (and without complications from additional impurities). Our strategy is to generate amorphous SiO₂ structures using classical molecular dynamics and use these structures as input to study the electronic properties.

We limit the number of atoms in the cell to a value close to 100 in order to be able to generate results in a reasonable time and with a good level of accuracy. Consequently, we used a rectangular supercell of graphene containing 32 carbon atoms within the area $8.52 \text{ \AA} \times 9.84 \text{ \AA}$; these dimensions correspond to the optimized unit cell for isolated graphene (i.e., $a = 2.46 \text{ \AA}$). Our method to generate the SiO₂ substrate follows a procedure described in detail in a previous publication by Leed *et al.*,²⁵ where it was shown that an amorphous SiO₂ structure could be generated with the correct density of defects, including three-fold-coordinated silicon atoms and nonbridging oxygen atoms. In brief, we start by generating a periodic cell with the experimental density of amorphous SiO₂, 2.2 g/cm. The x and y dimensions of the cell are chosen to match the dimensions of the 32 atom graphene supercell. The z direction is chosen to contain 78 atoms in the SiO₂ slab. The coordination is corrected by running a classical molecular dynamics simulation to anneal the seed structure at high temperature (2500 K) for 110 ps with a time step of 0.001 ps. We use the Feuston–Garofalini potential²⁶ for SiO₂ to describe the atomic interactions as implemented in the General Utility Lattice Program (GULP).²⁷ This potential was tested before and produces amorphous SiO₂ surfaces in good agreement with experimental information (i.e., density of defects at surfaces, materials density, and coordination).^{25,28} We create the surface by removing the periodic boundary condition (PBC) in the z direction only. This open surface slab was further annealed from high temperature until the cell was properly equilibrated. Finally, as expected from SiO₂ surfaces exposed to ambient conditions, we terminate all remaining oxygen dangling bonds with hydro-

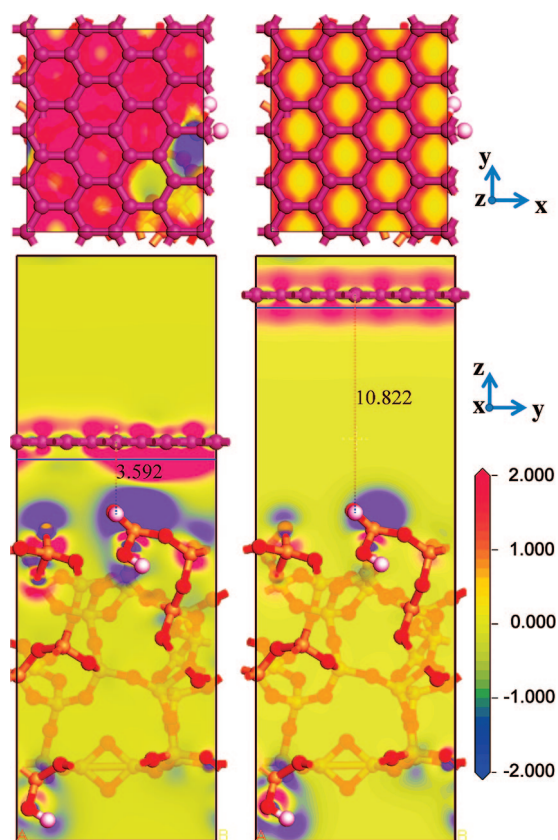


Figure 4. Atomic configuration used for the *ab initio* calculations. The left panel corresponds to the graphene sheet at the minimum energy distance, the right panel to a configuration with graphene at a larger distance. The contours of the charge transfer (left panel) are color coded to signify the magnitude of the electron excess after bringing the graphene and SiO₂ together.

gen and silicon dangling bonds with hydroxyls. One example of a SiO₂ slab generated in this way is shown in Figure 4 together with a flat graphene sheet in proximity to the substrate surface atoms. The distance (d) between substrate and graphene is defined as the minimum distance between the SiO₂ and graphene, as indicated. As such, this distance is an underestimation of the average distance that would be typically measured. We next relax the atomic positions of the SiO₂ substrate, but not those of the graphene sheet. Thus, in this first study, we ignore the effect of observed corrugations in the graphene^{14,29} as it relaxes to contact the rough SiO₂ surface. Our theoretical model therefore focuses on purely chemical charge transfer effects.

All electronic structure calculations reported in this work were done using density functional theory (DFT) with a plane wave basis set as implemented in the Vienna *Ab Initio* Simulation Package (VASP).^{30–33} The core electrons were treated with a frozen projector augmented wave method.^{34,35} The exchange and correlation potential was treated with a generalized gradient approximation using the Perdew–Burke–Ernzerhof (PBE) functional.^{36,37} The plane wave energy cutoff determining the basis set size was set to 282.8 eV, and the

Brillouin zone was sampled with Monkhorst–Pack³⁸ grid of $4 \times 4 \times 1$ for the convergence calculation and $12 \times 12 \times 1$ for density of states calculation. We tested our results with the local density approximation, and the overall conclusion of our work is not affected by our computational method. Self-interaction correction schemes that describe with greater accuracy the electron affinity are computationally very demanding and cannot be done with such a large unit cell.

The adsorption energy, that is, the energy gained when putting graphene on the substrate, is evaluated as the difference between the total energy of the combined graphene/substrate system and the sum of the total energies of the isolated parts. In all the three SiO₂ substrate configurations considered, we found a shallow minimum at $d = 3.6$ Å, with an average cohesive energy of 1 meV/Å². These two values are in good agreement with experiments on clean samples¹⁴ and also estimations of the adsorption (assembly) energy per unit area based on the energy needed to corrugate the graphene sheets.

The number of electrons (Q) transferred from the SiO₂ substrate to graphene and the net induced surface charge density n_0 in graphene are shown in Figure 5a as a function of the distance between the graphene sheet and the substrate. In all three substrate cases (SiO₂–1, SiO₂–2, and SiO₂–3), we observe intrinsic n-doping of the graphene sheets with a strong dependence on the distance when graphene is close to the surface. In Figure 5b, we display the calculated profile of the charge density redistribution (λ) produced after bringing together the graphene sheet and the SiO₂. At every position in the z direction of the cell (perpendicular to the surface), we integrate the difference in the plane of the electronic charge densities between the combined system and the sum of the isolated components. Positive values indicate that, after graphene is combined with the substrate, there are more electrons in that region. To determine the total charge transfer to graphene per unit area, we integrate the profile in the region between the two vertical dotted lines corresponding to the graphene sheet. We observe that one of the substrates (SiO₂–1) produces a slightly larger charge transfer than the others.

Another interesting effect is that the extra charge density gained by graphene is always accompanied by a reduction of the charge density at the position of the carbon atoms. This is seen as a negative dip in a plot of the charge difference λ versus d at the center of the graphene sheet. The effect has also been found by oth-

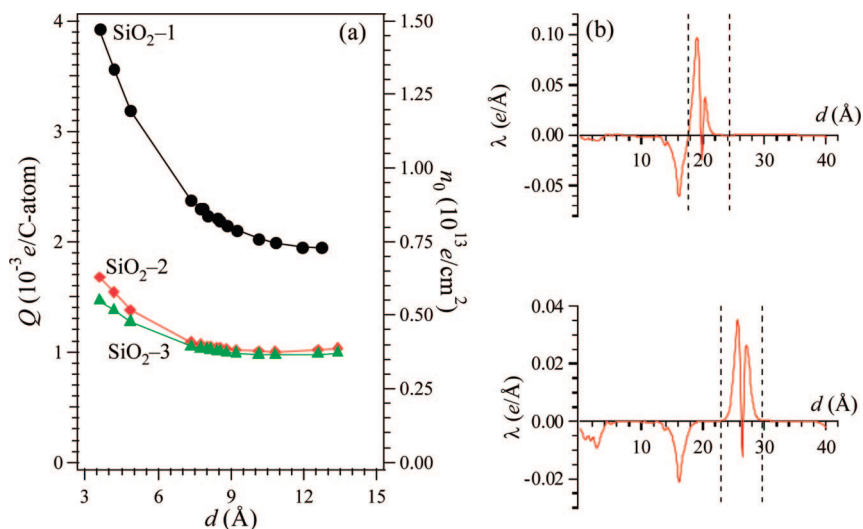


Figure 5. (a) Number of electrons Q transferred from the SiO₂ substrate to graphene and the net induced surface charge density n_0 as function of the distance d between graphene and the substrate. Results are shown for the three atomic substrate configurations considered in this work. It should be noted that the charge density does not extrapolate to zero due to the periodic boundary conditions imposed on our calculations. (b) Excess charge per unit distance λ plotted versus the distance d along the direction perpendicular to the SiO₂/graphene interface. The top panel shows the case when the graphene sheet is at the equilibrium distance with respect to the substrate; the bottom panel refers to the case when the sheet is at a large distance (10.8 nm) away. The vertical dashed lines indicate the formal boundary chosen for the SiO₂/graphene interface (left) and the outside boundary of the graphene (right).

ers in studies of metal adatom adsorption on graphene.³⁹ Calculations made for an isolated graphene sheet with extra electrons added to the cell show the same charge redistribution effect as we calculate here. We are currently doing further studies on this effect which could possibly be produced by a change in the screening due to the additional charge.

The work function of a substance is the energy necessary to remove an electron to infinity from the Fermi level. Within DFT, this is estimated as the energy difference between the electron at the Fermi level and the electrostatic potential at a far removed location in the vacuum region. In this way, we determined the work function of graphene and that of the three substrates considered in this work. The definition of these work functions is indicated schematically in Figure 6; the figure also defines the electrostatic problem to be solved to determine the relation between V_{Dirac} and the SiO₂ surface state density (Appendix). It should be noted that, in our model, the Fermi level in SiO₂ is pinned to the position of surface states near the conduction band edge. These states therefore define the work function of the clean substrate. For the substrates studied here, we find small differences in the SiO₂ work function: SiO₂–1 ($W = 3.03$ eV), SiO₂–2 ($W = 3.36$ eV), and SiO₂–3 ($W = 3.41$ eV). The variations observed between the three substrates are representative of the variations expected due to the random nature of the amorphous SiO₂ structure. However, all of them have a significantly smaller work function than graphene ($W_g = 4.23$ eV). Importantly, this difference explains the experimental observation (Figure 2) of intrinsic n-doping

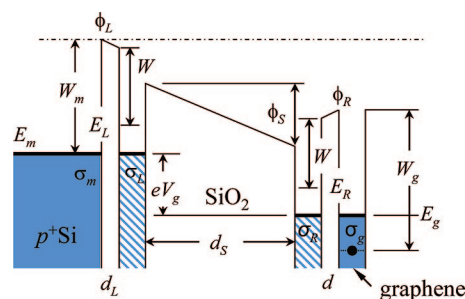


Figure 6. Potential diagram for a back-gated graphene FET on SiO₂/Si substrate. The p⁺Si gate is on the left, and the graphene is on the right; the gate dielectric (SiO₂) has a thickness $d_s = 300$ nm. According to our *ab initio* results, the work function for SiO₂, due to surface states, is $W = 3.03$ eV; the work function of graphene is $W_g = 4.23$ eV, and the density of surface states on the SiO₂ is $\beta = 4.5 \times 10^{12}$ eV⁻¹ cm⁻². An expression for the Dirac voltage as a function of gate potential V_g is derived in the Appendix. In the figure, E_L and E_R are the changes in the Fermi level of the surface states on the left and on the right, respectively, of the SiO₂ substrate. E_m is the Fermi level on the doped Si and E_g the Fermi level on graphene; σ 's denote the different surface charge densities; ϕ_S and d_s are, respectively, the potential drop and the width of the SiO₂ layer; ϕ_L , ϕ_R , d_L , and d are the potential drops and the width of the small gaps between the different regions that are assumed to be zero in the derivation of the model (see the Appendix).

when graphene is in contact with *clean* SiO₂. The origin of the relatively smaller work function of substrate SiO₂-1 is the presence of a particular configuration with low binding energy surface states.

The charge transfer observed is the origin of the attraction between the SiO₂ substrate and graphene. However, at the equilibrium distance of $d = 3.6$ Å, there is an additional charge rearrangement effect that is shown in the color-coded charge contours of Figure 4. These are charge puddles. The inhomogeneities of the charge density of the ionic SiO₂ substrate produce a rearrangement of the in-plane charge density of graphene. This effect is apparent in the left panel of Figure 4. We expect this in-plane charge rearrangement to have a significant influence on the transport properties of the first graphene layer deposited on SiO₂, such as proposed recently.⁹ Further additional graphene sheets overlaying the sheet in contact with the SiO₂ will be screened by the first one, and the effect of the substrate on the more distant sheets will be smaller.

We are now in a position to comment on the experimental Dirac voltage obtained from the gate voltage sweeps. Using eq 2, the experimental value for the oxide thickness $d_s = 300$ nm (Figure 6) and the average density of surface states obtained from our *ab initio* calculation (*i.e.*, $\beta = 4.5 \times 10^{12}$ eV⁻¹ cm⁻²), we obtain $V_{\text{Dirac}} \sim -74$ V, quite close to the measured value of -50 V (Figure 3b). Using eq 1 for the gate bias dependence of the device, we obtain an experimental value for $n_0 = 4.3 \times 10^{12}$ e/cm², in excellent agreement with the theory (*cf.* Figure 5a). Many other samples were also studied. Although the time required for the FETs to evolve from p-type to n-type behavior differed, we al-

ways found the Dirac voltage in the range $V_g \sim -30$ to -50 V.

Finally, as discussed briefly above, we observe that, as the device is cooled in high vacuum from 200 to 25 °C, V_{Dirac} increases rapidly from -50 V to a new steady-state value at -30 V (Figure 3b). As a first attempt to explain this temperature effect, we assumed a simple model where the temperature associated with Fermi occupation of the states is varied and the charge density is adjusted self-consistently. This simple model produced behavior opposite to experimental observation; that is, the calculated Dirac voltage became more negative. We are thus forced to consider what additional complications must be added to our model to explain the experimental observation. The best we can offer at this time is that complications due to the conformation of the graphene sheet to the rough topology of the substrate have not been included. We intentionally neglected this effect in order to focus on chemical charge transfer in the simplest model (*i.e.*, flat graphene). We are currently initiating more sophisticated calculations, including the bending of the graphene sheet, to understand how the sheet curvature may affect the chemistry between SiO₂ and graphene and the T dependence of the Dirac voltage.

CONCLUSIONS

We have shown experimentally that degassed graphene FETs on SiO₂ behave as an n-type system. From the experimental point of view, this follows from the observation that, after long-term (20 h) degassing in vacuum at 200 °C, the Dirac peak is positioned at large negative gate voltages ($|V_g| > 10-50$ V). This behavior was observed in six samples. On the other hand, p-type behavior is observed initially (before degassing). We identify (1) the initial *positive* Dirac voltage (p-type behavior) with chemical charge transfer from gaseous dopants found in common laboratory air and (2) the final *negative* Dirac voltage (n-type behavior) in degassed FETs with intrinsic behavior. Ignoring the conformation of graphene to the underlying SiO₂ surface roughness (rms ~ 3 nm), our theoretical calculations can explain the observed intrinsic n-type behavior by the relatively low value of the work function of SiO₂ which is associated with a Fermi level pinned in surface states that form just below the conduction band. The experimental net surface charge density in vacuum-degassed graphene FETs supported on Si/SiO₂ substrates is found to be $n_0 \sim 4 \times 10^{12}$ e/cm², in good agreement with our electronic calculations of the surface state density at the SiO₂/graphene interface. However, our current model calculations for flat graphene cannot explain the experimental observation of a decrease in the excess charge density with decreasing temperature. Further experimental and theoretical work will be necessary to elucidate this phenomenon.

EXPERIMENTAL DETAILS

Bottom-gated field effect transistors (FETs) using graphene as the conducting channel were fabricated by micromechanical cleavage of highly oriented pyrolytic graphite (HOPG) into few-layer graphene films (Grade ZYH HOPG, SPI Supplies, West Chester, PA). These films were then transferred by tape (Scotch Tape, 3M) from the HOPG onto degenerately doped Si(100) substrates ($\rho \sim 3 \times 10^{-4} \Omega \cdot \text{cm}$) with a 300 nm overlayer of thermally grown SiO_2 .⁴⁰ The Si substrate also served as a back gate electrode. Metal pads based on evaporated Cr (5 nm) followed by Au (100 nm) were used to contact the source and drain ends of the FET. These metals were electron-beam evaporated onto the graphene through square holes in a TEM grid (SPI SLIM Bar Indexed Grid, SPI Supplies, West Chester, PA). While viewing the graphene film through an optical microscope, the grid was first positioned appropriately over the film using a micromanipulator. The grid consisted of a 10×10 array of $115 \times 115 \mu\text{m}^2$ square holes separated by $\sim 10 \mu\text{m}$ bars. A more detailed description of our shadow mask procedure will be given elsewhere.

The graphene FET on Si was then placed in a chip carrier, and the device was connected *via* wire-bonded leads between pads on the substrate and chip carrier. The number of layers (N) in the graphene film was determined by micro-Raman scattering using the shape of the "2D" Raman band at $\sim 2700 \text{cm}^{-1}$ and the intensity of the G-band scattering at $\sim 1585 \text{cm}^{-1}$.^{41,42} The essential idea behind the Raman characterization of N is threefold: (1) the G-band intensity is linear in N ; (2) an $N = 1$ (graphene) film can be easily recognized by the narrow Lorentzian shape of the 2D Raman band; and (3) at least one $N = 1$ film must be present on the same substrate, so that other films can be identified *via* their G-band intensity. This is accomplished by a simple translation of the microscope stage, while all optics remain fixed. Here, we present results on one representative sample that was demonstrated by Raman scattering to be an $N = 1$ graphene film.

Chip carriers were placed in a socket supported within a stainless steel tube (2.5 cm diameter \times 30 cm long) that was connected to a gas manifold and turbo-molecular vacuum pump; the tube was inserted into a furnace and could be evacuated to 5×10^{-7} Torr. A type-K thermocouple was mounted on the chip carrier near the Si substrate to monitor the local temperature. Electrical measurements were made using a programmable voltage source and digital voltmeter/ammeter (Model 2400, Keithley Instruments, Inc., Cleveland, OH) interfaced to a computer *via* LabVIEW (National Instruments Co., Austin, TX). The measurements involved the application of a small constant source–drain voltage $V_{ds} = 1 \text{mV}$, while monitoring the resultant source–drain current (I_{ds}) as a function of the gate voltage (V_g); the source–drain resistance is computed as $R_{ds} = V_{ds}/I_{ds}$.

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APPENDIX

In this Appendix, we will derive an expression for the dependence of the net charge density on the graphene as a function of the applied V_g . The derivation assumes that a surface charge develops at the $\text{SiO}_2/\text{graphene}$ and $\text{SiO}_2/p^+\text{Si}$ interfaces due to surface states on the SiO_2 . A schematic drawing of the electrostatic diagram for the FET device is shown in Figure 6. If we neglect the small potential drops in the narrow gaps on both sides of SiO_2 , energy conservation requires

$$\begin{aligned} W_m &= W + E_L \\ eV_g + E_L &= \phi_s + E_R \\ W_g &= W + E_R + E_g \end{aligned} \quad (\text{A3})$$

where the meaning of the different potentials are indicated in the figure. Using Gauss' law on both sides of the device, we obtain

$$\begin{aligned} \sigma_R + \sigma_g &= \frac{\epsilon\epsilon_0\phi_s}{ed_s} \\ \sigma_L + \sigma_m &= -\frac{\epsilon\epsilon_0\phi_s}{ed_s} \end{aligned} \quad (\text{A4})$$

If we assume that the density of states of the surface states is constant, the charge densities at the surface of SiO_2 and in the graphene sheet are given by

$$\begin{aligned} \sigma_R &= e\beta E_R \\ \sigma_g &= -\frac{e}{\pi(\hbar v_F)^2} E_g^2 \equiv -\alpha E_g^2 \end{aligned} \quad (\text{A5})$$

Combining these equations, we can obtain an expression that provides the Fermi level in graphene, E_g , as a function of device parameters

$$\left(\frac{e^2\beta d_s}{\epsilon\epsilon_0} + 1\right)(W_g - W - E_g) - \frac{e^2\alpha d_s}{\epsilon\epsilon_0} E_g^2 = eV_g + W_m - W \quad (\text{A6})$$

The Dirac voltage is defined as the voltage for which the charge in graphene is zero (*i.e.*, $E_g = 0$)

$$V_{\text{Dirac}} = \left(\frac{e\beta d_s}{\epsilon\epsilon_0} + 1\right) \frac{(W_g - W)}{e} - \frac{(W_m - W)}{e} \quad (\text{A7})$$

Using this definition, the equation for the Fermi level of graphene is given by

$$-\left(\frac{e^2\beta d_s}{\epsilon\epsilon_0} + 1\right) E_g - \frac{e^2\alpha d_s}{\epsilon\epsilon_0} E_g^2 = e(V_g - V_{\text{Dirac}}) \quad (\text{A8})$$

Using the density of surface states determined from our *ab initio* calculations, the coefficient for the term linear in E_g is more than 10 times smaller than the coefficient for the quadratic term. As a consequence, the linear term in eq A6 can be neglected and eq 1 is obtained.

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